Method of forming submicron contacts and vias in an integrated circuit

Patent Number: ☐ EP0780894, A3
Publication date: 1997-06-25
Inventor(s): LIOU FU-TAI (US); ZAMANIAN MEHDI (US)
Applicant(s): SGS THOMSON MICROELECTRONICS (US)
Requested Patent: JP9181180
Application Number: EP19960309299 19961219
Priority Number(s): US19950574659 19951219
IPC Classification: H01L21/768
EC Classification: H01L21/768B2D
Equivalents: ☐ US5847460
Cited patent(s): DE4340419; EP0369953; US4472240

Abstract

A method of forming a small geometry via and a structure formed thereby in which an opening is formed partially through an insulating layer (16), sidewalls (26) formed in the opening, and the remaining insulating layer etched to expose an underlying conductive region (14). Alternatively a thick oxide (36') is formed in the opening and etched to form sidewalls (38). Alternatively, an etch stop layer (42) is formed between the insulating layer and conductive region and an opening formed exposing the etch stop layer. A sidewall spacer film (46) is formed over the insulating and etch stop layers. The etch stop and spacer layers are etched thereby forming a contiguous layer. Alternatively a second insulating layer (56) is formed over the etch stop layer (54). An opening is formed then the spacer film (66) is formed. An etch exposes a portion of first insulating layer (16). A second opening is formed in the first insulating layer.